Impact of Current Limiters of Grid-Following Inverters on Power System Dynamic Performance

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***Abstract*—During grid disturbances that require the injection of large currents, Inverter-Based Resources (IBRs) are particularly vulnerable to thermal stress and potential damage. Current limiters prevent damaging the semiconductors but also reduce the ability of IBRs to support the grid during and after the clearance of a severe contingency. There is the need, thus, for effective current-limiting strategies that can simultaneously ensure inverter protection and maintain system support. This work proposes a new promising current-limiting solution, compares it with state-of-the-art current-limiting strategies though a comprehensive case study, and discusses possible advantages of different solutions in different fault scenarios.**

***Index Terms*—Current limiter, Grid-Following (GFL) inverter, voltage support, frequency metric, Inverter-Based Resource (IBR).**

I. Introduction

A. Motivation

As IBRs displace traditional synchronous generators [1]–[3], the limited thermal tolerance of inverter semiconductor components can become critical during grid disturbances that demand high current injection, such as fault conditions. In particular, the inverter must limit its output current to prevent thermal damage. However, excessive current limitation can be critical, as adequate current injection is required during certain grid conditions, such as reactive power support for voltage regulation [4]. Thus, the implementation of adequate current-limiting strategies is critical to ensure both system stability and component protection. This work focuses on the design of a current limiter that provides a good trade-off between IBR protection and power system dynamic performance.

B. State of the art

This section reviews the most prevalent *Direct Approach* [5] current limiting strategies documented in the literature, with a specific focus on Grid-Forming (GFM) control applications. The authors in [6] present three current limiting strategies: the *Instantaneous Limiter* with a square boundary, the *Magnitude Limiter* featuring a circular boundary, and the *Fixed-Angle Limiter*. Furthermore, the performance of the Magnitude and Fixed-Angle limiters under symmetrical disturbances is evaluated. The transient stability analysis of the *Magnitude Limiter* is further investigated in [7], while the authors in [8] illustrate the fault recovery analysis for the *Fixed-Angle Limiter*. Circular current limiters in GFMs are also investigated in [9] to enhance low voltage ride-through capability. Current-limiting GFM inverters are also analysed in [10] in terms of small-signal analysis. In [11], the two most common Priority-Based Limiter are analyzed in a transient stability analysis: the *d-priority* and *q-priority* strategies. Similar strategies that either prioritise d-q components, or active-reactive power support, can be also found in [12]. The impact of current limiting modes on the transient stability of hybrid parallel systems, comprising both Grid-Following (GFL) and GFM inverters is investigated in [13].

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C. Contribution

This work provides three main contributions to the existing state of the art. In particular, we provide:

- a systematic comparison of current-limiting strategies for GFL inverters, which is currently lacking in the scientific literature, mostly focusing in GFM inverters;
- a novel current-limiting strategy that takes into account real-time voltage measurements;
- a quantitative evaluation of current limiters performance, using conventional voltage and frequency quality metrics.

II. Current limiters

The output current of an inverter can be either constrained by directly manipulating the reference signals, i.e., *direct limiting approach*, or *indirectly*, by adjusting related quantities, such as voltages or impedances. In a conventional grid-following (GFL) inverter employing a synchronous reference frame (SRF) control scheme, the direct (d) and quadrature (q) current references $i_{d,\mathrm{ref}}$ and $i_{q,\mathrm{ref}}$ are obtained from the active and reactive power set-points. A current-limiting stage is now required before the current references are used to generate appropriate modulations signals to control the pulse-width modulation (PWM) stage, for a safe operation of inverters. Accordingly, the reference signals must be bounded to ensure that the maximum allowable current $I_{\max}$ of the inverter is not exceeded, namely:

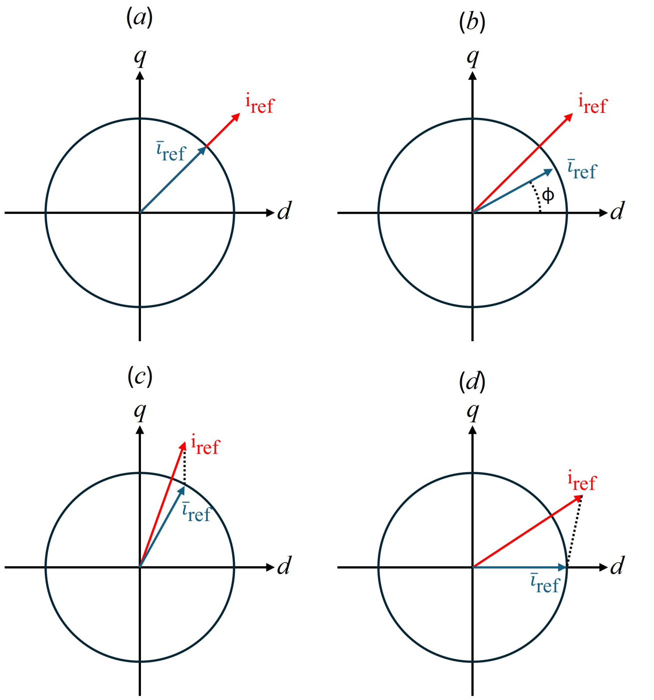

Fig. 1. Graphical illustration of a magnitude limiter 1.(a), fixed angle limiter 1.(b), d-priority limiter when the d-axis current magnitude is smaller than $I_{\max}$ 1.(c), and a d-priority limiter when the d-axis current magnitude is greater than $I_{\max}$ 1.(d).

$$\sqrt{\bar{\imath}_{d,\text{ ref}}^2 + \bar{\imath}_{q,\text{ ref}}^2} = |\bar{\imath}_{\text{ref}}| \le I_{\max}, \tag{1}$$

where $|\bar{\imath}_{\text{ref}}|$ is the current magnitude after the limiting block and $I_{\max}$ denotes the maximum allowable current.

A. Trajectory-based current limiters

Trajectory-based strategies represent the most straightforward methodology to current limiting in power electronic inverters [14]. These strategies identify an admissible operating region for the reference current vector, within the stationary or synchronous reference frame. The two most common geometric constraints are the square and the circular regions:

- **Square Boundary:** The reference current components are limited independently along each axis, such that $|\bar{\imath}_{d,q,\text{ref}}| \le \frac{I_{\max}}{\sqrt{2}}$. This strategy is simple to implement, and it is guaranteed that $|\bar{\imath}_{\text{ref}}| \le I_{\max}$, but it also limits some currents that do actually satisfy constraint (1). For this reason, this limiting strategy is not considered in the remainder of this work.
- **Circular Boundary:** The admissible operating region is now defined as a circle with a radius equal to the maximum inverter current, $I_{\max}$. A common realization of a circular boundary is the *magnitude limiter*, whereby current vectors outside the admissible region are projected onto the boundary without altering their phase angle, as shown in Fig. 1.(a).

Components of the magnitude limiters may be mathematically expressed as:

$$\begin{cases} \bar{\imath}_{d,\text{ref}} = \dfrac{I_{\max}}{|i_{\text{ref}}|} \cdot i_{d,\text{ref}} \\ \bar{\imath}_{q,\text{ref}} = \dfrac{I_{\max}}{|i_{\text{ref}}|} \cdot i_{q,\text{ref}} \end{cases} \tag{2}$$

so that both the d and q components are proportionally scaled, preserving the phase of the current vector while limiting its magnitude.

B. Priority-based current limiters

Priority-based limiting strategies extend the concept of admissible regions by introducing a hierarchy between the current components. When the current reference vector exceeds the predefined boundary, the limiter does not merely saturate the current magnitude; instead, it prioritises either the d- or q-axis current to meet specific operational requirements. In GFL inverters employing SRF control, the d and q components are typically decoupled to regulate active power (P) and reactive power (Q) independently. Consequently, determination of a specific priority significantly affects the inverter's performance during saturation.

1) Fixed-angle limiters: Fixed-angle limiters still consider a circular region, but now, when the limit is exceeded, the current vector is projected into the admissible region with an *a priori* chosen angle ϕ, as exemplified in Fig. 1.(b).

$$\begin{cases} \bar{\imath}_{d,\text{ref}} = I_{\max}\cos(\phi) \\ \bar{\imath}_{q,\text{ref}} = I_{\max}\sin(\phi). \end{cases} \tag{3}$$

Therefore, ϕ serves as a tuning parameter for power allocation; for instance, increasing ϕ enhances the q-axis reference, thus favoring reactive power over active power during current saturation events.

2) d-, q-priority limiters: In d-priority limiters, the inverter gives priority to the d-axis component. Two main subcases can be distinguished, as follows.

1) In the event that the current vector exceeds the admissible region while its d-component remains within the maximum current limit ($|\imath_{d,\text{ref}}| \le I_{\max}$), the vector tip is shifted vertically, as depicted in Fig. 1.(c). This approach preserves the original d-axis reference while clipping the q-component to the boundary of the circular constraint, as described by:

$$\begin{cases} \bar{\imath}_{d,\text{ref}} = i_{d,\text{ref}} \\ \bar{\imath}_{q,\text{ref}} = \text{sgn}(i_{q,\text{ref}})\sqrt{I_{\max}^2 - \bar{\imath}_{d,\text{ref}}^2}; \end{cases} \tag{4}$$

2) Alternatively, if the current vector exceeds the admissible region and its d-component alone is already greater than the maximum allowed current ($|i_{d,\text{ref}}| > I_{\max}$), the vector is restricted to the d-axis, as illustrated in Fig. 1.(d). Consequently, the q-component is set to zero and the d-component is clipped to $I_{\max}$, preserving its original sign:

$$\begin{cases} \bar{\imath}_{d,\text{ref}} = \text{sgn}(i_{d,\text{ref}})I_{\max} \\ \bar{\imath}_{q,\text{ref}} = 0 \end{cases} \tag{5}$$

In general, this type of limiter is designed to ensure that active power injection never drops to zero during the limiting process.

The logic of q-priority limiters is the same as that of d-priority strategies, but roles are swapped and priority is given to the q component.

C. Proposed Current Limiter

The limiters considered this far operate in an *a priori* manner, without taking into account the dynamic evolution of the system during the event that triggers the current limitation. Thus, we propose a novel GFL current limiting strategy that takes into explicit account the real-time measured voltage at the Point of Common Coupling V_{PCC}, as we expect that embedding this information in the design of the current limiter may support the decision of how to best limit the current.

For this purpose, we now consider a non-linear function as follows to select the reference value $\bar{\imath}_{q,\mathrm{ref}}$ as a function of V_{PCC}, as follows:

$$i_q = \begin{cases} I_{\max}, & V_{\mathrm{PCC}} < 0.5 \\ I_{\max}\left[1 - \left(\frac{V_{\mathrm{PCC}} - 0.9}{0.4}\right)^{\alpha}\right], & 0.5 < V_{\mathrm{PCC}} < 0.9 \\ 0, & V_{\mathrm{PCC}} > 0.9, \end{cases} \quad (6)$$

where α is a parameter that can be used to leverage the flexibility of the designed current limiter and decide which component of the current should be given higher priority.

Figure 2 shows the behaviour of the reference signal $\bar{\imath}_{q,\mathrm{ref}}(\alpha, V_{\mathrm{PCC}})$ as a function of parameter α. The limiting logic is divided into three distinct V_{PCC} operating ranges, each defining a specific priority for the current injection:

- $V_{\mathrm{PCC}} \geq 0.9\,\mathrm{pu}$: the inverter delivers only the d-axis current component ($\bar{\imath}_{q,\mathrm{ref}} = 0$), as the voltage levels are within a non-critical range.
- $0.5\,\mathrm{pu} \leq V_{\mathrm{PCC}} < 0.9\,\mathrm{pu}$: the q-axis current reference $\bar{\imath}_{q,\mathrm{ref}}$ is defined as a function of the measured voltage V_{PCC}, according to the value of α. Values of α greater than one prioritise the q-component injection, thereby allocating greater current headroom for reactive power support. Conversely, values of α smaller than 1 give priority to the d-component, favouring active power delivery.
- $V_{\mathrm{PCC}} < 0.5\,\mathrm{pu}$: the inverter injects the maximum allowable q-axis current, as these voltage levels are considered critical for the system stability.

Remark: The reference value for $\bar{\imath}_{d,\mathrm{ref}}$ can be derived as $\sqrt{I_{\max}^2 - \bar{\imath}_{q,\mathrm{ref}}(\alpha, V_{\mathrm{PCC}})^2}$.

III. Case Study

The dynamic performance of the current limiters described in the previous sections are evaluated and compared using extensive simulations carried out using the power system simulator Dome [15], [16]. The current limiters are implemented using the Python programming language and integrated them into a GFL inverter model. The case study is based on a modified version of the IEEE 9-bus test network [17] with two synchronous generators (SGs) and one IBR with the GFL inverter. The impact of the analysed limiters on the system's dynamic performance is evaluated considering three scenarios:

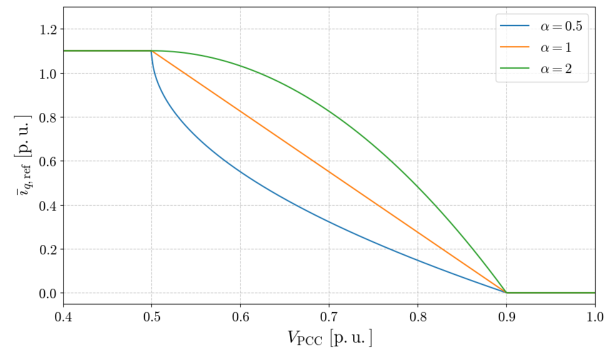

Fig. 2. q-axis current characteristic for $\alpha = 0.5$, 1, and 2. By increasing α it is possible to modify the voltage dependent reactive current injection.

- **Scenario 1:** A three-phase short circuit at bus 9 with a duration of 100 ms, resulting in a voltage drop at the Point of Common Coupling (V_{PCC}) within the range of 0.5 to 0.9 pu.
- **Scenario 2:** A three-phase short circuit at bus 9 with a duration of 100 ms, where V_{PCC} falls below 0.5 pu.
- **Scenario 3:** The sudden loss of a synchronous generator.

The first two scenarios are characterized by an over-frequency condition, corresponding to a *mild* and a *severe fault* condition, respectively. The fault duration is the maximum allowed by the Irish Transmission System Operator (TSO) for high voltage networks, and according to the grid code, the IBR must always remain connected to the grid. Conversely, the last scenario induces an under-frequency event.

The objective of this comparison is to evaluate the impact of the described limiters on key system dynamic metrics. These include the average voltage at the PCC during the disturbance, the Center of Inertia (COI), frequency Zenith for over-frequency transients, and the Nadir for under-frequency events. Additionally, the analysis considers the maximum Rate of Change of Frequency (RoCoF) and the overall settling time for frequency recovery. In the following tables, we denote the magnitude limiter as the "no-priority" case.

A. Scenario 1: Mild over-frequency condition

In this case, the parameter α influences the inverter response; specifically, higher values of α enhance the q-axis current injection, thereby providing greater reactive power support during the disturbance.

The trajectory of limited currents for all cases are depicted in Figs. 3.(a) and 3.(b) for the d and the q components, respectively, while performance metrics are shown in Table I. The the last three rows of the table refers to the performance of the proposed current limiter, for different values of α. The fixed-angle limiter (with ϕ equal to $45°$) provides the best results, both in terms of frequency and voltage support, while the proposed limiter with $\alpha = 2$ is the second best.

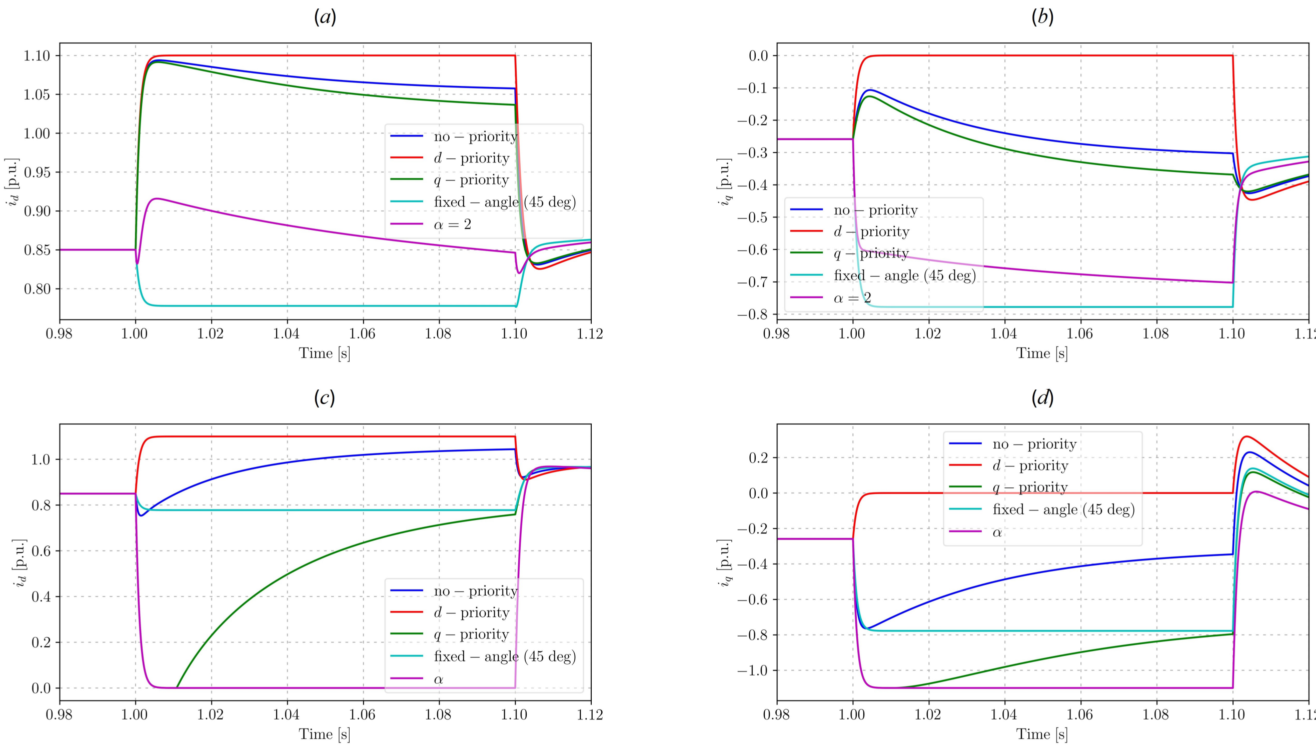

Fig. 3. Graphical illustration of the limited currents according to different limiting strategies in the mild fault scenario (a) and (b), where only the proposed current limiter with $\alpha = 2$ is shown for the sake of simplicity, and in the severe fault scenario (c) and (d).

TABLE I
COMPARISON OF SYSTEM DYNAMIC METRICS FOR DIFFERENT LIMITING STRATEGIES IN THE MILD FAULT CONDITION

Limiting Logic	**Average** V_{PCC} [pu]	**Zenith** [Hz]	**Max. RoCoF** [Hz/s]	**Recovery Time** [s]
no-priority	0.67	50.35	2.75	2.68
d-priority	0.63	50.38	2.94	2.79
q-priority	0.68	50.34	2.68	2.65
Fixed-Angle ($\phi = 45°$)	**0.77**	**50.24**	**1.86**	**2.07**
$\alpha = 0.5$	0.69	50.33	2.66	2.63
$\alpha = 1$	0.72	50.31	2.43	2.54
$\alpha = 2$	0.72	50.27	2.08	2.35

TABLE II
COMPARISON OF SYSTEM DYNAMIC METRICS FOR DIFFERENT LIMITING STRATEGIES IN THE SEVERE FAULT CONDITION

Limiting Logic	**Average** V_{PCC} [pu]	**Zenith** [Hz]	**Max. RoCoF** [Hz/s]	**Recovery Time** [s]
no-priority	0.27	50.53	3.48	3.58
d-priority	0.26	50.54	3.44	3.59
q-priority	0.31	50.52	3.32	3.54
Fixed-Angle ($\phi = 45°$)	0.32	50.50	3.30	3.52
α	**0.38**	**50.42**	**2.46**	**3.33**

B. Scenario 2: Severe over-frequency condition

For V_{PCC} levels below 0.5 pu, the inverter response becomes independent of α, as the device is restricted to exclusive reactive current injection. Thus, the proposed solution is indicated as α for short. The trajectories of the currents is illustrated in Figs. 3.(c) and 3.(d) for the d and the q components, respectively. Performance in terms of key system dynamic metrics are shown in Table II. Results show that the proposed current limiter provides the best performance.

C. Scenario 3: Under-frequency condition

This scenario evaluates the system response following the outage of a SG. As this contingency triggers an under-frequency event, the proposed limiter is expected to enhance frequency stability for lower α values. Under such conditions, the control logic prioritizes the d-axis current component, thereby maximizing active power support. In under-frequency scenarios, the frequency Nadir is a more critical performance indicator than the Zenith. Furthermore, RoCoF is excluded from this specific analysis; in fact, given the extremely low inertia of the system, the resulting RoCoF values exceed safe operational limits and are incompatible with standard grid stability requirements.

Results in Table III confirm that frequency metrics marginally improve when the limiter adopts lower values of α. However, differences are substantially negligible. This behaviour is mainly due to the relatively small voltage deviation following the loss of an SG: since V_{PCC} remains near 0.9 pu, the current reference characteristics for different α values are very close, as illustrated in Fig. 2.

TABLE III
COMPARISON OF SYSTEM DYNAMIC METRICS FOR DIFFERENT α VALUES OF THE PROPOSED LIMITER IN THE UNDER-FREQUENCY SCENARIO

Parameter value	**Nadir** [Hz]	**Recovery Time** [s]
α = 0	49.49	1.25
α = 0.1	49.49	1.26
α = 1	49.48	1.26

D. *Discussion of Results*

The inverter implementing q-axis priority yields best overall performance in terms of PCC voltage support across all analysed scenarios. This is primarily due to the increased reactive power injection facilitated by this limiting strategy. Regarding the proposed limiter, selecting $\alpha > 1$ emerges as the most effective configuration for enhancing voltage stability. As per the frequency metrics, the optimal configuration depends on the specific disturbance: in under-frequency scenarios, selecting $\alpha < 1$ provides slightly better performance by prioritising active power injection, although the observed improvements are marginal. Conversely, in over-frequency events, prioritising the q-axis current component yields superior results; therefore, selecting $\alpha > 1$ represents the most effective strategy overall. Overall, selecting $\alpha = 2$ appears to provide the best trade-off. This value allows maintaining reactive power headroom while guaranteeing continued active power injection into the grid and voltage support during disturbances.

IV. CONCLUSIONS AND FUTURE WORK

This work proposes a novel current-limiting strategies for GFL inverters and compares it with existing current-limiting approaches described in the literature. Differently from conventional solutions, the proposed strategy takes into account the real-time value of the voltage at the point of common coupling. Results obtained through extensive simulations show that in different fault scenarios the proposed current limiter always provides the best — or the second best — performance, according to several voltage/frequency indicators.

Future work will extend the proposed work in the following directions: (i) consider the interaction of several inverters and the impact of current-limiter strategies (ii) implement a real-time adaptive control of α (e.g., as a function of the measured grid frequency) to improve the performance of the current limiter; (iii) consider grid-forming converter architectures; and (iv) consider unbalanced operating conditions and asymmetrical grid disturbances.

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