Comparison of Different PLL Implementations for Frequency Estimation and Control

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***Abstract*—Accurate and fast-responding Phase-Locked Loops (PLLs) are crucial for the implementation of primary frequency controllers of non-synchronous generation and energy storage devices that are connected to the grid through power electronic converters. PLLs are primarily designed to synchronize a converter to the grid and their ability to estimate frequency deviations is a design-dependent, not necessarily optimized byproduct. The goal of the paper is to establish which design better filters noise and reduces numerical spikes after sudden variations of the voltage at the terminal ac bus of the converter. To this aim, the paper compares five well-assessed PLL implementations through a standard IEEE benchmark system considering both contingencies and noise.**

***Keywords*—Distributed energy resources, frequency control, frequency estimation, frequency-locked loop, phase-locked loop.**

I. Introduction

A. Motivation

The utilization of PLL devices is becoming more and more important as the penetration of power electronic converters in electric energy systems increases. PLLs primary purpose is to synchronize the converters to the grid. A byproduct of such synchronization is that the PLL is able to estimate frequency deviations, which can be utilized to implement frequency regulation. However, the primary purpose of the PLL is not frequency estimation. So far, it has not been fully discussed which is, among the many possible PLL implementations, the most adequate PLL design for frequency control. The focus of this paper is to compare a variety of well-assessed PLL designs and study their ability to estimate local frequency deviations.

B. Literature Review

The main purpose of the PLL is the synchronization of power electronic converters to a three-phase ac grid. Since, in turn, a PLL is a closed-loop controller with inclusion of a filter, its implementation is not unique. In the literature, the main focus so far has been to propose and test PLL designs that properly filter harmonics, compensate unbalanced conditions and reduce the delay and the error with which the phase is tracked.

Recent publications have recognized the impact of PLLs in the regulation provided by non-synchronous devices [1], [2], but also the potential instabilities that these devices can cause to electronic converters [3]–[5]. Reference [6] shows how the delays and fast flux dynamics introduced by PLLs can affect the ability of non-synchronous devices to properly regulate the frequency. On the other hand, the noise of frequency signals can be filtered and is, generally, less harmful [7].

There are several PLL solutions specifically designed for power electronic converters. The Synchronous Reference Frame PLL (SRF–PLL) is likely the simplest and the most commonly utilized scheme [8]. Other configurations are aimed at improving the SRF–PLL to reduce noise, distortions and internal parameter uncertainties. Within this category, we cite the Lag PLL (Lag–PLL) [9]; the Low-Pass Filter PLL (LPF–PLL) [10]; the Enhanced PLL (E–PLL) [11]; and the Second-order Generalized Integrator (SOGI) with Frequency-Locked Loop (FLL) [12]–[14].

A drawback of PLL noise filtering is the introduction of delays in the estimation of the phase and, consequently, of frequency deviations. With this regard, alternative solutions to the PLL for grid synchronization aimed at improving the compromise between speed and noise filtering have been proposed in the literature. For example, in [15], the authors propose an algorithm in the discrete time-domain based on the well-known Kalman Filter.

Despite some drawbacks, PLLs are the simplest and most widely-used phasor synchronization devices. For this reason, we focus exclusively on PLLs and compare a variety of implementations to define the proper trade-off between accuracy and responsiveness. With this aim, we need an *ideal* signal – i.e., a signal virtually free of noise and delay – to which compare the frequency estimation of the PLLs. This signal is based on the Frequency Divider Formula (FDF), recently proposed by the authors in [16] and further developed in some following works [6], [17], [18].

C. Contributions

The contributions of this paper are twofold.

- The models of five common PLL designs suitable for the conventional transient stability analysis which is based on quasi-steady state voltage phasors in polar coordinates.
- A thorough comparison of the dynamic performance of five different PLL implementations for the estimation of frequency deviations.

The five PLL implementations considered in the paper are: SRF–PLL, Lag–PLL, LPF–PLL, E–PLL, and SOGI–FLL.

978-1-5386-0517-2/18/$31.00

D. Organization

The remainder of this paper is organized as follows. Section II describes the basic elements that compose a generic PLL scheme as well as the five PLL configurations considered in this work. Section III outlines the FDF proposed in [16] and that is utilized in this paper to obtain noise-free bus frequency signals to which the PLLs frequency estimations are compared. Section IV presents a case study based on the WSCC 9-bus system and a variety of contingencies and noises that allow to test the dynamic response of the five PLL implementations considered in Section II. Finally, Section V draws conclusions and outlines future work.

II. Phase-Locked Loop Configurations

The input signals of PLLs for power electronic applications are the three-phase voltages at the bus where the converter is connected. These voltages are projected onto the dq reference frame and the $v_q(t)$ component is tracked and minimized. This ensures that the converter is synchronized with the ac grid frequency at the point of connection and utilizes $v_d(t)$ as phase reference.

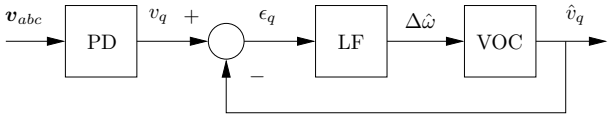

Fig. 1: Basic scheme of a PLL.

A basic scheme of a PLL is depicted in Fig. 1. This scheme is composed of three main parts, as follows.

i. The Phase Detector (PD), which measures the vector of three-phase voltage at the bus of connection, $\boldsymbol{v}_{abc}(t)$. The voltage is then converted from abc representation into $\alpha\beta$- and dq-reference frames, and the q-axis component $v_q(t)$ is computed.

ii. The Loop Filter (LF), which takes the error $\epsilon_q(t)$ between the measured q-axis voltage, $v_q(t)$, and the one estimated by the PLL, $\hat{v}_q(t)$. While there exist several different configurations of the LF, they are generally based on a perfect tracking controller, e.g., a PI.

iii. The Voltage Oscillator Control (VOC), which takes the bus frequency deviation, $\Delta\hat{\omega}(t)$ and provides the estimation of the bus voltage q-axis component $\hat{v}_q(t)$. The VOC typically consists of a pure integrator to avoid steady-state errors in $\hat{v}_q(t)$, and impose that, in steady-state, $v_q(t) = 0$.

For transient stability studies, such as the one carried out in this paper, $\boldsymbol{v}_{abc}(t)$ is not available, as the model is based on a balanced, fundamental frequency and quasi-steady state phasor representation of network branches and devices. The transformations operated within the PD cannot thus be explicitly implemented. Depending on the network model, in fact, either the components $v_d(t)$ and $v_q(t)$ or the polar representation in term of voltage magnitude $v(t) = |v_d(t) + jv_q(t)|$ and phase angle $\theta(t) = \angle(v_d(t) + jv_q(t))$ are directly available at the point of connection of the converter.

In the following, we use exclusively polar coordinates for bus voltage phasors. This is equivalent to assume that the output of the PD is the voltage phase angle $\theta(t)$. In fact, $v_q(t) = v(t)\sin(\theta(t))$, which shows that, in steady-state, the condition $v_q(t) = 0$ is equivalent to $\theta(t) = 0$.

The signal measurements and transformations performed in the PD, however, are not instantaneous. For this reason, the PD is assumed to be a *pure delay* in the fundamental frequency model utilized in this paper. Hence, the output of the PD is $v_{q,\tau}(t) = v_q(t-\tau)$ or, using polar coordinates $\theta_\tau(t) = \theta(t-\tau)$.

The VOC is a pure integrator. For this reason, its input signal has to be in steady-state the rate of change of the controlled PLL signal. Since we have shown above that tracking $v_q(t)$ is equivalent to track the phase angle $\theta(t)$ of the bus voltage phasor $\bar{v}(t)$, the input quantity of the VOC is the rate of change of such angle or, in other words, an estimation of the frequency deviation $\Delta\hat{\omega}(t)$ at the bus where the PLL is connected.

To obtain the actual frequency at the bus, one has to add to $\Delta\hat{\omega}(t)$ the fundamental frequency of the system. This is a constant, say ω_0, if synchronous machines rotor speeds are referred to the synchronous frequency of the system, namely:

$$\dot{\delta}_i(t) = \Omega_b(\omega_i(t) - \omega_0) \ , \tag{1}$$

where $\delta_i(t)$ and $\omega_i(t)$ are the rotor angle and angular speed, respectively, of machine i, and Ω_b is the value of synchronous frequency of the system in rad/s (e.g., 314.15 rad/s in a 50 Hz grid).

In simulations, referring machine speed deviations to the frequency of the Centre of Inertia (COI) is also useful to avoid the drift of machine angles, which leads to time consuming simulations in long term stability analysis [19]. For these reasons, the COI is implemented in most commercial software tools for the dynamic simulation of power systems, e.g., Eurostag and PSS/E. If the frequency of the COI is used, then (1) has to be rewritten as:

$$\dot{\delta}_i(t) = \Omega_b(\omega_i(t) - \omega_{\mathrm{COI}}(t)) \ , \tag{2}$$

where

$$\omega_{\mathrm{COI}}(t) = \frac{\sum_i^n M_i\omega_i(t)}{\sum_i^n M_i} \ , \tag{3}$$

where M_i is the inertia constant of the i-th synchronous machine. In this paper, (2) is utilized as the rotor angle equation of synchronous machines and, hence, the frequency estimated by the PLL is computed as:

$$\hat{\omega}(t) = \omega_{\mathrm{COI}}(t) + \Delta\hat{\omega}(t) \ . \tag{4}$$

Note that, in standard transient stability models, $v_q(t)$ and the phase angle $\theta(t)$ are algebraic variables. Therefore, the computation of its derivative by the LF is prone to jumps, spikes and/or numerical issues in the event of discontinuities such as line outages or faults that may occur in the system. For this reason the estimation of the frequency deviations through the PLLs can show numerical issues, which are duly discussed in the case study.

The remainder of this section provides a brief description of five typical PLL configurations that are used in transient stability studies.

A. SRF–PLL

The SRF–PLL is currently one of the simplest and most commonly used PLLs configurations [8], [18]. A fundamental-frequency model of a SRF–PLL is depicted in Fig. 2, where the PD is modeled as a pure delay; the LF is a PI controller; and the VOC is implemented as an integrator.

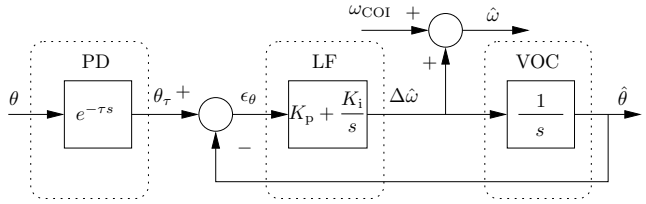

Fig. 2: Scheme of the SRF–PLL.

The interested reader can find in [18] a comprehensive transient stability study on the performance of a variety of non-conventional primary frequency control devices in transmission systems when their local input signal is provided by a SRF–PLL.

B. Lag–PLL

Figure 3 shows a variation of the SRF–PLL presented above. In this configuration, referred to as Lag–PLL, a low-pass filter is added in the LF prior to the PI regulator [9]. The aim of the low-pass filter is to reduce the sensitivity of the PLL to noises and to prevent numerical issues when computing $\Delta\hat{\omega}(t)$.

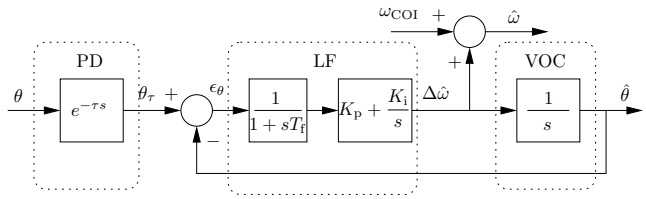

Fig. 3: Scheme of the Lag–PLL.

C. LPF–PLL

Another possible implementation of the PLL is shown in Fig. 4, originally proposed in [10] and called LPF–PLL. Despite its name, the implementation of the LF proposed in [10] resembles more of a lead-lag block. The purpose of this block is to filter noises and possible numerical issues that may arise when computing $\Delta\hat{\omega}(t)$, while preventing the addition of large delays in the process.

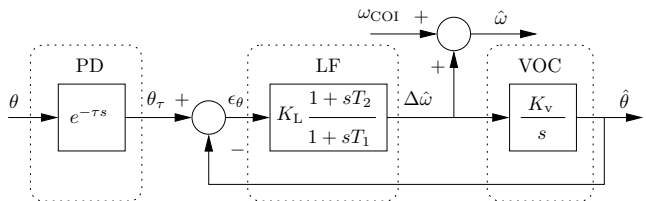

Fig. 4: Scheme of the LPF–PLL.

D. E–PLL

Figure 5 shows the single-phase implementation of the E–PLL that was originally proposed in [11]. The LF is composed of a PI regulator as for the SRF–PLL. The main differences reside in the PD, as it is implemented as a combination of the pure delay τ and an Adaptive Notch Filter [20]. The E–PLL can be designed to be robust against noise, distortions and uncertainties of internal parameter setting, and to be able to adaptively follow frequency variations. The main drawback of the E–PLL is its relative slow response, since the estimation process takes more than one cycle.

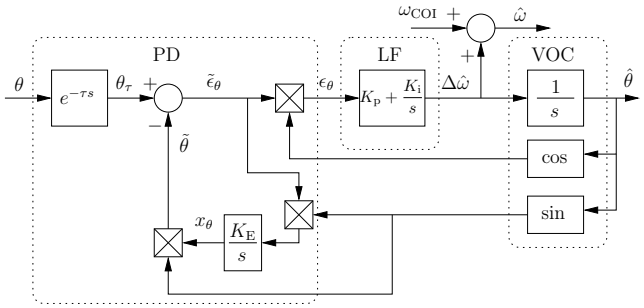

Fig. 5: Scheme of the E–PLL.

E. SOGI–FLL

The last PLL configuration discussed in this paper is depicted in Fig. 6 [12]. This implementation consistently differs from the previous PLLs illustrated, as it includes a SOGI, i.e., an adaptive filter structure whose input signal is the resonant frequency $\tilde{\omega}$ [13], and a FLL, which adapts $\tilde{\omega}(t)$ [14]. In [12], the authors propose a cross-feedback, multiple SOGI–FLL tuned at different frequencies to estimate the sequence components of $v(t)$ under severe distortion conditions. In this paper, we consider the single SOGI-FLL configuration to estimate $\hat{\omega}(t)$.

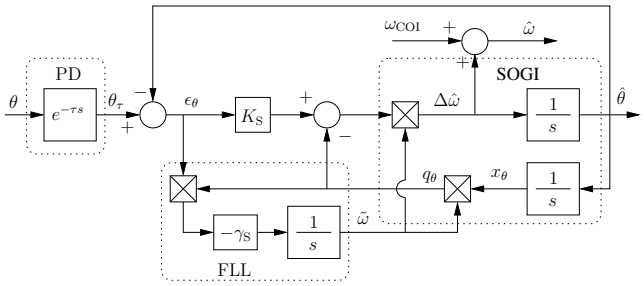

Fig. 6: Scheme of the SOGI–FLL.

III. Frequency Divider Formula

In [16], a new technique to estimate local frequency variations at every bus of a given network is proposed. This technique, called *Frequency Divider Formula* (FDF), relates such local variations with synchronous machine rotor speeds and Phasor Measurement Unit (PMU) measurements by means of the augmented admittance matrix of the system, as formulated below.

$$\Delta\boldsymbol{\omega}_B = -\mathbf{B}_{BB}^{-1} \cdot \mathbf{B}_{BG} \cdot \Delta\boldsymbol{\omega}_G \tag{5}$$

where $\Delta\boldsymbol{\omega}_B$ are the bus frequency deviations; $\Delta\boldsymbol{\omega}_G$ are the synchronous machine rotor speed deviations; $\mathbf{B}_{BB}$ is the extended network susceptance matrix with inclusion of the internal reactances of the synchronous machines; and $\mathbf{B}_{BG}$ is incidence susceptance matrix at the bus where generators are connected to the network.

For computational efficiency purposes, it is advisable to formulate (5) as an acausal expression, as follows:

$$\mathbf{0} = \mathbf{B}_{BB} \cdot \Delta\boldsymbol{\omega}_B + \mathbf{B}_{BG} \cdot \Delta\boldsymbol{\omega}_G \tag{6}$$

The main advantage of the above formulation is that it does not require computing $\mathbf{B}_{BB}^{-1}$. While $\mathbf{B}_{BB}$ is typically highly sparse, in fact, its inverse in an almost fully dense matrix. This is particularly relevant when large systems are considered. Moreover, the frequency estimation provided by (6) is free of numerical issues such as the spikes after discontinuous events that characterize the frequency signals provided by PLLs and PMUs.

The expressions in (5) and (6) are certainly accurate for standard transient stability models and simulations, as thoroughly discussed in [16]–[18]. A validation of the FDF considering Electromagnetic Transient (EMT) models and hardware-in-the-loop PMU devices is presented in [21], [22]. Experimental results confirm that the set of hypothesis and simplifications, the most relevant of which is that fast electromagnetic dynamics are neglected, that lead to the definition of (6) are consistent and do not lead to any significant error.

IV. Case Study

This section compares the performance of the five PLL configurations discussed in this paper, and benchmarked against the *ideal* frequency estimation of the FDF. The well-known WSCC 9-bus system is considered for simulations. The system includes three synchronous machines, loads and transformers, and six transmission lines, as well as primary frequency and voltage regulation and an Automatic Generation Control (AGC). Figure 7 shows the scheme of the 9-bus system. All static and dynamic data can be found in [23].

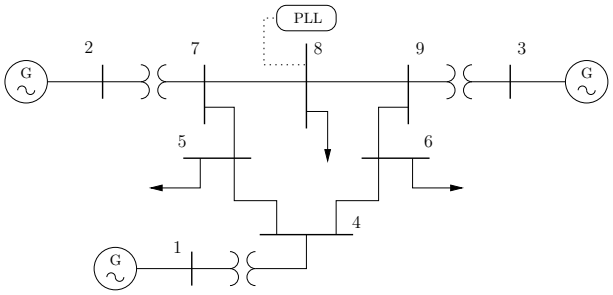

Fig. 7: WSCC 9-bus test system.

The case study considers two scenarios. In Subsection IV-A, a three-phase fault is simulated to study the accuracy of each PLL configuration following large and fast frequency variations. Then, Subsection IV-B discusses the sensitivity of the PLLs to noise in their input signal, i.e., in the bus voltage angles.

All simulations and plots presented in this section were obtained using the software tool DOME [24] running on a 4 core 2.60 GHz Intel© Core i7™ with 8 GB of RAM.

A. Three-phase Fault

In this subsection, a three-phase fault is simulated at $t = 0.5$ s at bus 7. The fault is cleared 80 ms after its occurrence by opening the line connecting buses 7 and 5. The step of the time integration process is 1 ms, and every step is solved by using the dishonest Newton-Raphson method [25]. Finally, the integration method used is the implicit trapezoidal formula.

The parameters of the PLL schemes depicted in Figs. 2–6 are listed in Table I. Such parameters have been tuned by means of trial-and-error techniques in order to obtain the best performance for each configuration. The time delay τ is zero for all configurations.

TABLE I: Values of the parameters of the PLL controllers.

PLL	Parameter	Value	Unit
SRF–PLL	K_p	0.1	–
	K_i	0.05	–
LPF–PLL	K_L	1.0	–
	T_1	0.5	s
	T_2	0.01	s
	K_v	1.0	–
E–PLL	K_E	30.0	–
	K_p	0.30	–
	K_i	0.1	–
Lag–PLL	T_f	0.01	s
	K_p	0.5	–
	K_i	0.1	–
SOGI–FLL	K_S	2.0	–
	γ_S	0.5	–

The frequency at the load bus 8 is estimated by each of the PLL configurations discussed in the paper, and compared to the estimation provided by the FDF, and the trajectories are shown in Figs. 8 (SRF–PLL, LPF–PLL and E–PLL) and 9 (Lag–PLL and SOGI–FLL). Additionally, the absolute estimation errors ϵ_ω between each PLL estimation and the FDF signal are depicted in Fig. 10.

The most accurate frequency estimations are achieved with the LPF–PLL and the Lag–PLL, showing the latter the highest spikes of the two at the fault occurrence and the line opening. The SRF–PLL shows the lowest spikes during the two discontinuous events, but it also shows high ϵ_ω. Finally, the E–PLL and the SOGI–FLL show the worst performance overall, since their signals have the highest spikes (1.025 and 1.17, respectively), and ϵ_ω during the first swings.

B. Noise

PLLs are known to be sensitive to the noise of the measured signal, i.e., the bus voltage angle. While the level of noise in transmission systems is generally small, this noise is of higher relevance in distribution systems due to the proximity of loads, unbalances, harmonics of power electronic converters, etc. This subsection considers a scenario where noise is applied to all bus voltage angles of the 9-bus system. Such a noise is modeled as a Ornstein-Uhlenbeck's process with Gaussian distribution [26].

The frequency at the load bus 8 is estimated by means of each PLL configuration, and the trajectories are shown in

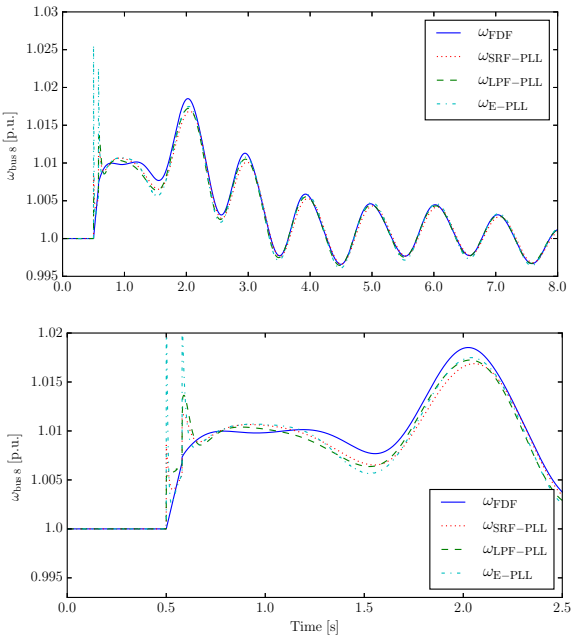

Fig. 8: Frequency of bus 8 estimated with the FDF, SRF–PLL, LPF–PLL and the E–PLL during a three-phase fault.

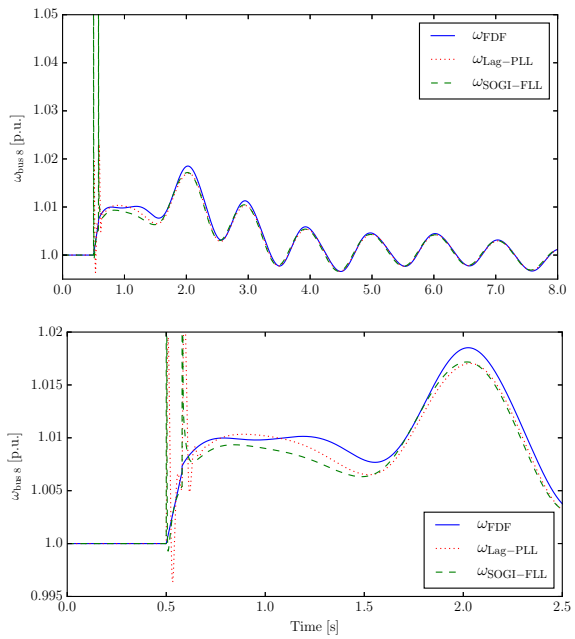

Fig. 9: Frequency of bus 8 estimated with the FDF, Lag–PLL and the SOGI–FLL during a three-phase fault.

Fig. 11, whereas the absolute frequency errors ϵ_ω are depicted in Fig. 12. Note that, for the short time simulated, the noise does not have impact on the synchronous machine rotor speeds, and thus the frequency estimated by the FDF used to compute ϵ_ω is equal to 1 pu. The parameters of the different PLLs utilized to obtained the plots in Figs. 2–6 are the same as those listed in Table I.

The LPF–PLL is the least sensitive to the noise applied to the bus voltage angles, followed by the SRF–PLL. The Lag–PLL shows a smooth estimation, but the latency inserted by its low-

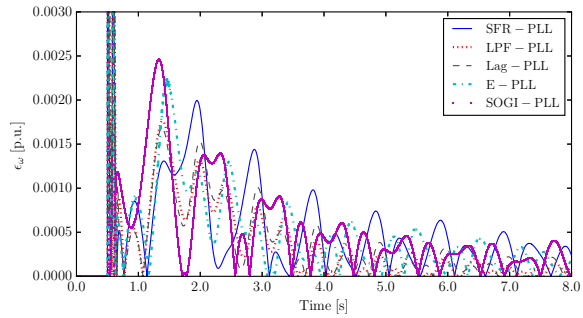

Fig. 10: Absolute errors of the frequency estimated at bus 8 during a three-phase fault.

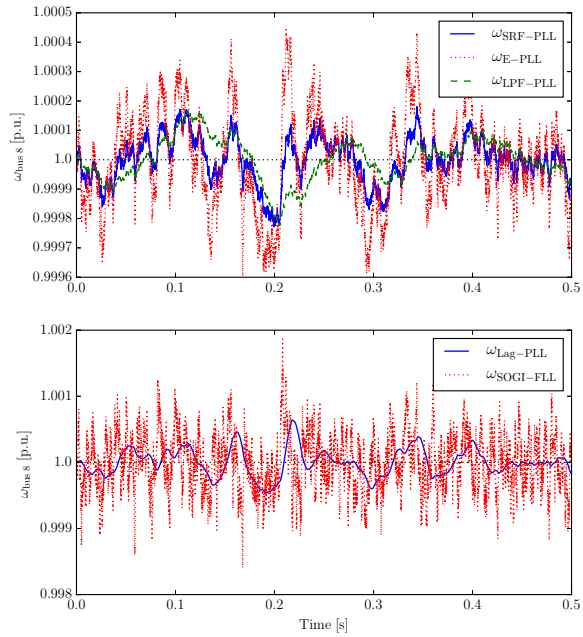

Fig. 11: Frequency estimated at bus 8 under the presence of noise in the PLLs input signal.

pass filter block leads to greater ϵ_ω. Finally, the E–PLL and the SOGI–FLL are the most sensitive to jitter, showing the latter the worst performance overall.

V. Conclusions

The paper compares the accuracy and the sensitivity to noises present in the input signal of five PLL configurations used for frequency estimation, namely the SRF–PLL, LPF–PLL, Lag–PLL, E–PLL and the SOGI–FLL. The comparison is based on simulations performed considering several scenarios, large disturbances and relatively high levels of noise on the well-known WSCC 9-bus, 3-machine test system. Simulation results allow concluding that the LPF–PLL has the best performance overall, as it provides the most accurate frequency estimation after fast and large frequency variations caused by contingencies such as faults and line outages, and it also shows the least sensitivity to noise present in the bus voltage angles. An overall good performance is also achieved by the commonly-used SRF–PLL and the Lag–PLL. Finally, the worst accuracy, and the highest sensitivity to noise are observed from the E–PLL, and to a greater extent, from the SOGI–FLL. Future work will focus on

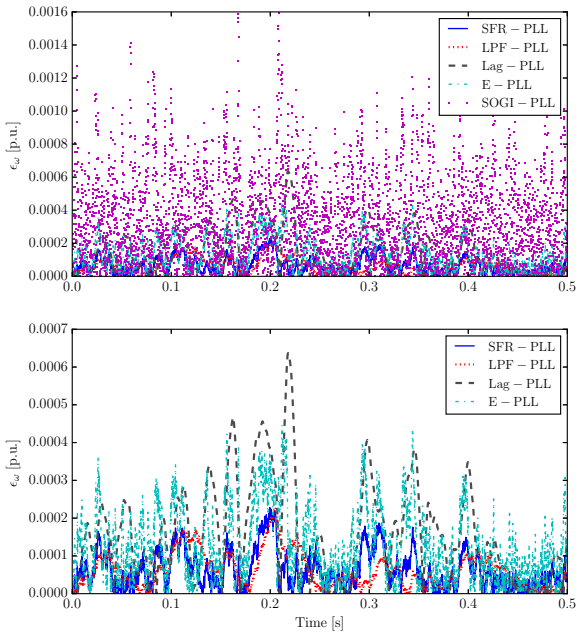

Fig. 12: Absolute error of the frequency estimated at bus 8 under the presence of noise in the PLLs input signal.

the comparison of the LPF–PLL with other grid synchronization solutions such as the one proposed in [15]. The technique discussed in [5] to evaluate the impact of harmonics on the estimation of the fundamental frequency deviations of PLLs will be also considered.

ACKNOWLEDGMENTS

This material is based upon works supported by the European Commission, by funding Á. Ortega and F. Milano, under the RESERVE Consortium (grant No. 727481). F. Milano is also funded by the Science Foundation Ireland, under Investigator Programme, Grant No. SFI/15/IA/3074, and a beneficiary of the EC Marie Skłodowska-Curie CIG No. PCIG14-GA-2013-630811.

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This Article is part of a project that has received funding from the **European Union's Horizon 2020 research and innovation programme under grant agreement Nº727481**